TITLE OF THE INVENTION

ACTIVE MATRIX TYPE FLAT-PANEL DISPLAY DEVICE

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FIELD OF THE INVENTION

The present invention relates to an active matrix type flat-panel display device with light emissive elements such as EL (electro luminescent) elements or light nonemissive elements such as liquid crystal elements arranged two dimensionally in matrix and sequentially driven by means of respective drive thin film transistors (TFTs).

DESCRIPTION OF THE RELATED ART

An active matrix type flat-panel display device with light emissive elements and respective drive TFTs which are two dimensionally arranged along X-axis and Y-axis in matrix is known. In such device, the drive TFTs of the respective picture elements are sequentially scanned by column-selecting transistors (TFTs) and line-selecting transistors (TFTs). Each of the column-selecting transistors which are sequentially turned on by means of an X-axis shift register is connected to each column. The line-selecting transistors are prepared for the respective drive TFTs and sequentially turned on by means of a Y-axis shift register so that the line-selecting transistors connected to each line are simultaneously turned on.

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According to such the device, since each of the column-selecting transistors has to drive all the drive TFTs on that column, it is necessary to use as a high power transistor as for this column-selecting transistor. Particularly, in case that the light emissive elements are constituted by high speed elements such as EL elements, high speed switching operation will be required by using extremely high power TFTs.

These high power TFTs for the column-selecting transistors result time constant determined by their large gate capacitance and on-resistance of circuits connected to the gates of the column-selecting transistors to extremely increase and thus cause rise edges and fall edges of selection signals applied to these respective gates to delay by a certain period ΔT. Therefore, a selection signal to be applied to one column-selecting transistor will overlap on a next selection signal to be applied to the next column-selecting transistor for the delay time ΔT causing the both of the neighboring column-selecting transistors to simultaneously keep on during this period ΔT. As a result, a video signal for a light emissive element positioned at a certain column and a certain line will be strayed into a next light element positioned at the neighboring column and the same line causing picture quality of the display device to deteriorate.

SUMMARY OF THE INVENTION

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It is therefore an object of the present invention to provide an active matrix type flat-panel display device whereby picture quality can be greatly improved by preventing overlap between selection signals of neighboring columns or lines from occurring.

According to the present invention, an active matrix type flat-panel display device includes a flat substrate, a plurality of light emissive elements arranged two dimensionally along columns and lines on the flat substrate, a plurality of selection switches formed on the flat substrate, for sequentially selecting the light emissive elements to provide video signals thereto, selection signal generation circuits for providing selection signals which drive the selection switches in sequence so as to two dimensionally scan the light emissive elements, and a selection signal control circuit for preventing the selection signals to be outputted from the selection signal generation circuits for a predetermined period of time so as to eliminate overlap between the selection signals.

Thus, overlap between selection signals of neighboring columns or lines can be prevented from occurring causing picture quality to be greatly improved.

Preferably, the selection switches consist of column-selecting transistors arranged for the respective columns of the light emmisive elements, and line-selecting transistors arranged for the respective light emissive elements.

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The column-selecting transistors and the line-selecting transistors may be formed by thin film transistors.

It is preferred that the selection signal generation circuits include a first shift register for providing the selection signals in sequence to the column-selecting transistors, and a second shift register for providing the selection signals in sequence to the line-selecting transistors.

Preferably, the selection signal control circuit includes a mask signal generation circuit for producing a mask signal with a duration of time which corresponds to the predetermined period of time, and a logic circuit for shortening a duration of the selection signals by the duration of the mask signal.

The above-mentioned predetermined period time may be equal to 5 to 50 % of a half clock cycle.

The light emissive elements may consist of organic electro luminescent elements, non-organic electro luminescent elements, ferroelectric liquid crystal elements or field emission diodes.

Further objects and advantages of the present invention will be apparent from the following description of the preferred embodiments of the invention as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 schematically shows a part of a preferred

embodiment of an active matrix type flat-panel display device according to the present invention;

Fig. 2 shows in detail a part of the display device of Fig. 1;

Fig. 3 shows a concrete constitution of a part of an X-axis shift register illustrated in Fig. 1;

Fig. 4 schematically shows a constitution of a clock signal and mask signal generation circuit;

Fig. 5 shows a concrete constitution of a mask signal generation circuit illustrated in Fig. 4;

Fig. 6 illustrates wave forms of a clock signal and a mask signal in the circuit of Fig. 4; and

Fig. 7 illustrates wave forms of various signals in the X-axis shift register of Fig. 3.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 schematically shows a part of a preferred embodiment of an active matrix type flat-panel display device according to the present invention.

As illustrated in the figure, the display device 10 has a flat display panel 11, an X-axis shift register 12 and a Y-axis shift register 13.

The flat display panel 11 has a substrate (not indicated) and a plurality of picture elements of light emissive elements which are two dimensionally arranged along X-axis and Y-axis in

matrix on the substrate. In this embodiment, the light emissive elements are constituted by organic EL (electro luminescent) elements. To the respective picture elements of the display panel 11, EL power and video signal are supplied. To the X-axis shift register 12, shift register power and an X-axis synchronous signal are supplied. To the Y-axis shift register 13, shift register power and a Y-axis synchronous signal are supplied.

Fig. 2 is an enlarged view of a circled portion in Fig. 1. As will be apparent from this figure, each of the picture elements P_{11}, P_{12}, ..., P_{21}, P_{22}, ...(illustrated by rectangles of broken lines) of the flat display panel 11 is constituted by two TFTs, a capacitor and an EL element.

Light emitting operation of the picture element P_{11} for example will be carried out as follows. When a selection signal x1 is outputted from the X-axis shift register 12 and a selection signal y1 is outputted from the Y-axis shift register 13, a column-selecting transistor (TFT) T_{x1} and a line-selecting transistor (TFT) T_{y11} are turned on. Thus, the video signal -VL is applied to a gate of a drive transistor (TFT) M_{11} via the transistors T_{x1} and T_{y11}. Accordingly, a current with a value depending upon the gate voltage -VL flows from the EL power supply through drain and source of the drive transistor M_{11} causing an EL element EL_{11} of this picture element P_{11} to emit light with a luminance corresponding to the voltage of the

video sighal -VL.

At a next timing, the X-axis shift register 12 puts off the selection signal x1 and outputs a selection signal x2. However, since the preceding gate voltage of the transistor M_{11} is held by a capacitor C_{11}, the picture element P_{11} will keep to emit light with a luminance corresponding to the voltage of the video signal -VL until this picture element P_{11} is selected again.

Fig. 3 shows a concrete constitution of a part of the X-axis shift register 12 in the embodiment of Fig. 1.

In the figure, two-input NAND circuits 21 and 22 constitute an wave-form shaping circuit for shaping wave form of an input signal to synchronize with basic clocks. The NAND circuit 21 is connected such that inverse basic clocks -CL having inverted phase with respect to the basic clocks are inputted into one input terminal of the NAND circuit 21 and that an output signal from the NAND circuit 22 is inputted into the other input terminal thereof. The NAND circuit 22 is connected such that a start pulse -SP with low level (L-level) will be inputted into one input terminal of the NAND circuit 22 and that an output signal from the NAND circuit 21 is inputted into the other input terminal thereof. The start pulse -SP is an X-axis synchronous signal which defines a start time of scanning toward the column direction.

The output terminal of the NAND circuit 21 is connected to

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an input terminal of a clocked inverter 26. This clocked inverter 26, clocked inverters 29 to 32 and inverters 33 to 37 constitute a shift register portion. Namely, each of stages of the shift register portion is formed as follows. The first stage is constituted by the clocked inverter 26, the inverter 33 connected to this clocked inverter 26 in series and the clocked inverter 29 connected to the inverter 33 in parallel but in opposite direction. The second stage is constituted by the clocked inverter 27, the inverter 34 connected to this clocked inverter 27 in series and the clocked inverter 30 connected to the inverter 34 in parallel but in opposite direction. The third stage is constituted by the clocked inverter 28, the inverter 35 connected to this clocked inverter 28 in series and the clocked inverter 31 connected to the inverter 35 in parallel but in opposite direction.

Inverters 38 to 43 and three-input NAND circuits 23 to 25 constitute a logic circuit portion for providing selection signals x1 to x3. An output terminal of the first stage of the shift register portion (output terminal of the inverter 33) is coupled with a first input terminal of the three-input NAND circuit 23 via the inverter 38. An output terminal of the second stage of the shift register portion (output terminal of the inverter 34) is coupled with a first input terminal of the three-input NAND circuit 24 via the inverter 39 and directly connected to a second input terminal of the NAND circuit 23.

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An output terminal of the third stage of the shift register portion (output terminal of the inverter 35) is coupled with a first input terminal of the three-input NAND circuit 25 via the inverter 40 and directly connected to a second input terminal of the NAND circuit 24.

Third input terminals of the NAND circuits 23 to 25 are connected to a mask signal generation circuit 41 shown in Fig. 4 to receive a mask signal -INL. An output terminal of the NAND gate 23 is coupled with a gate of a first column switching transistor T_{x1} via the inverter 41. An output terminal of the NAND gate 24 is coupled with a gate of a second column switching transistor T_{x2} via the inverter 42. An output terminal of the NAND gate 25 is coupled with a gate of a third column switching transistor T_{x3} via the inverter 43. Into sources of the switching transistors T_{x1} to T_{x3}, video signal -VL is applied.

The clocked inverter will be in active and operate as an inverter when L-level signal is applied to a clock input terminal shown at upper side and also H-level signal is applied to an inverted clock input terminal shown at lower side. Contrary to this, it will turn into high impedance state when H-level signal is applied to the clock input terminal and L-level signal is applied to the inverted clock input terminal. For example, since the clocked inverters 26 and 29 are constituted to receive opposite phase clocks with each other as

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shown in Fig. 3, the clocked inverter 26 will be in active when the clocked inverter 29 is in a high impedance state.

Fig. 4 schematically shows a constitution of a clock signal and mask signal generation circuit, Fig. 5 shows a concrete constitution of a mask signal generation circuit illustrated in Fig. 4, and Fig. 6 illustrates wave forms of a clock signal and a mask signal in the circuit of Fig. 4.

As shown in Fig. 4, the clock signal and mask signal generation circuit consists of a frequency divider 40 for dividing, by eight, frequency of a clock signal with eight-fold frequency, produced by a clock generator (not shown) to produce a basic clock signal CL, and a mask signal generation circuit 41 for producing a mask signal -INL from the clock signal with eight-fold frequency.

The frequency divider 40 may be constituted by a counter for counting the input clock signals to output the basic clock signal with H-level and L-level which alternate at every four input clock signals. Thus, the basic clock CL will have eight-fold pulse width in comparison with that of the input clock signal with eight-fold frequency as shown in Fig. 6.

As shown in Fig. 5, the mask signal generation circuit 41 consists of a three-bit counter 410 and a two-input NAND circuit 411 so as to count the input clock signal with eight-fold frequency for three clock cycles and provide an output signal with a one clock cycle duration of L-level. Thus, the

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mask signal -INL having a predetermined mask period of time MK can be obtained. As will be apparent from Fig. 6, this mask period MK is equal to a quarter of half clock cycle. The mask period MK according to this invention is not limited to a quarter of half clock cycle but can be determined to an optional period equal to or longer than an overlapped period ΔT of the selection signals. In practice, it is desired to select the mask period MK between about 5 and 50 % of the half clock cycle.

Fig. 7 illustrates wave forms of various signals in the X-axis shift register of Fig. 3. Hereinafter, operation of this embodiment will be illustrated in detail.

Output voltage A from the wave-form shaping circuit will be maintained at H-level when the start pulse of L-level -SP is not inputted. When the start pulse of L-level is inputted, the voltage A falls to L-level. As shown in Fig. 7, the start pulse -SP which is somewhat delayed due to a possible capacitance of input lead wires is shaped by the wave-form shaping circuit (21, 22) to synchronize with the basic clock CL.

When the voltage A falls to L-level, state of the clocked inverter 26 changes into active and thus output voltage B from the clocked inverter 26 will rise to H-level. Output voltage C from the inverter 33 (output from the first stage of the shift register) has an opposite phase wave form as that of the

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voltage B' due to the inverter 33.

When the state of the clocked inverter 26 changes into high impedance in next, since the clocked inverter 29 is in active, the voltage B is kept on H-level during this active period of the clocked inverter 29. Namely, the inverter 33 and the clocked inverter 29 constitutes a hold circuit.

Output voltage D from the clocked inverter 27 has an wave form delayed by a half clock cycle from that of the voltage B due to the operations of the clocked inverter 27 itself which simultaneously changes into active state with the clocked inverter 29 and of a hold circuit constituted by the inverter 34 and the clocked inverter 30.

Output voltage E from the inverter 34 (output from the second stage of the shift register) has an opposite phase wave form as that of the voltage D due to the inverter 34 and also has an wave form delayed by a half clock cycle from that of the voltage C.

Output voltage F from the clocked inverter 28 has an wave form delayed by a half clock cycle from that of the voltage D due to the operations of the clocked inverter 28 itself which simultaneously changes into active state with the clocked inverter 30 and of a hold circuit constituted by the inverter 35 and the clocked inverter 31.

Output voltage G from the inverter 35 (output from the third stage of the shift register) has an opposite phase wave form as that of the voltage

form as that of the voltage F due to the inverter 35 and also has an wave form delayed by a half clock cycle from that of the voltage E.

The voltage C is inverted by the inverter 38 and an inverted voltage H which is maintained H-level for a clock cycle is applied to a first input terminal of the three input NAND circuit 23. The voltage E having an wave form delayed by a half clock cycle from that of the voltage C is applied to a second input terminal of the NAND circuit 23. The mask signal -INL is applied to a third input terminal of the NAND circuit 23. The mask period MK of the mask signal -INL is determined to a certain period so that the falling edge of the selection signal x1 and the rising edge of the next selection signal x2 will not overlapped with each other.

Low-level duration of output voltage K from the NAND circuit 23 is shorter than that of the basic clock CL by the mask period MK. In other words, the output voltage K rises earlier than the basic clock CL by the mask period MK. This output voltage K is inverted by the inverter 41 to produce the selection signal x1.

The selection signal x1 is applied to the gate of the column-selecting transistor (TFT) T_{x1} which is formed by a N-channel field effect transistor. Thus, when the selection signal x1 rises to H-level, the transistor T_{x1} turns on.

The voltage E is inverted by the inverter 39 and an

inverted voltage I which is maintained H-level for a clock cycle is applied to a first input terminal of the three input NAND circuit 24. The voltage G having an wave form delayed by a half clock cycle from that of the voltage E is applied to a second input terminal of the NAND circuit 24. The mask signal -INL is applied to a third input terminal of the NAND circuit 24.

Low-level duration of output voltage L from the NAND circuit 24 is shorter than that of the basic clock CL by the mask period MK. In other words, the output voltage L rises earlier than the basic clock CL by the mask period MK. This output voltage L is inverted by the inverter 42 to produce the selection signal x2.

The selection signal x2 is applied to the gate of the column-selecting transistor (TFT) T_{x2} which is formed by a N-channel field effect transistor. Thus, when the selection signal x2 rises to H-level, the transistor T_{x2} turns on.

The voltage G is inverted by the inverter 40 and an inverted voltage J which is maintained H-level for a clock cycle is applied to a first input terminal of the three input NAND circuit 25. The voltage having an wave form delayed by a half clock cycle from that of the voltage G is applied to a second input terminal of the NAND circuit 25. The mask signal -INL is applied to a third input terminal of the NAND circuit 25.

Low-level duration of output voltage M from the NAND circuit 25 is shorter than that of the basic clock CL by the mask period MK. In other words, the output voltage M rises earlier than the basic clock CL by the mask period MK. This output voltage M is inverted by the inverter 43 to produce the selection signal x3.

The selection signal x3 is applied to the gate of the column-selecting transistor (TFT) T_{x3} which is formed by a N-channel field effect transistor. Thus, when the selection signal x3 rises to H-level, the transistor T_{x3} turns on.

Similar to this, the selection signals x1, x2, x3,... which are sequentially shifted by a half clock cycle with each other can be provided.

As described before, the wave forms of these selection signals x1, x2, x3,... shown in Fig. 7 by solid lines are ideal wave forms and actual wave forms applied to the respective gates of the transistors T_{x1}, T_{x2}, T_{x3},... may be as shown in Fig. 7 by broken lines. Namely, rising edges and falling edges of the selection signals may delay by a certain period ΔT due to the large gate capacitance of the transistors T_{x1}, T_{x2}, T_{x3},... and on-resistance of the inverters 41, 42, 43,....

However, according to the present invention, since the mask period MK during which no H-level signal is existed is provided between the selection signals, the switching transistor for example T_{x1} and the next switching transistor

for example T_{x2} never simultaneously be in on state.

Therefore, according to the present invention, picture quality of an active matrix type flat-panel display device can be greatly improved by preventing overlap between selection signals of neighboring columns or lines from occurring.

The light emissive elements may be constituted by non-organic EL elements, FLC (Ferroelectric Liquid Crystal) elements or FEDs (Field Emission Diodes) other than above-described organic EL elements.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.